line 13, change "; 3) the newly formed PN junction region 37" to --A PN junction region 37 is then formed which is --; line 14-15, d l te "and 4)"; line 18, after "bottom" insert -- intrinsic silicon surfaces to produce the top and bottom—; line 19, before "n w" insert --curved—.

Page 30, line 7, change "a" to --an--.; and change "producing a" to --to produce an--.

Page 32, lines16-17, delete "with reference to".

Page 65, line 6, change "sufficiently improved in" to --sufficient to improve--

IN THE DRAWINGS

Approval of the changes to Figs 4 & 5 , as noted in circles, are respectfully requested.

IN THE CLAIMS:

Please cancel all pending claims 1-65 and substitute therefor the following new claims:

--66. A solid state device comprising:

a solid state material substrate having a top surface;

a solid state material layer no more than 3 to 40 Angstroms thick, having at least one smooth major surface, and positioned on the top surface of the substrate;

at least a portion of the solid state material layer being metallurgically perfectly bonded uniformly to the at least a selected portion of the solid state device achieving thermochemical stability of a bonding interfacial region.

67. A solid state device as in claim 66 in which the solids state material layer has at least a number of the following features: a) having an atomically smoothed bottom surface; b) having a curved top surface; c) having an atomically liquid-smoothed gate bottom layer; c) made of purified material; d) made of strengthened material; e) accurate to one atomic layer in thickness; f) aged by liquid diffusion; f) fine-grained or subgrained; h) oriented grains or subgrains; i) narrow grains or subgrains; and j) stronger than unbonded material;

the number being selected from the group consisting of one, two, and three.

68. The device as in claim 66 in which the solid state material layer has a central portion of z ro width which is symmetrical with respect to a central bisecting plane thereof whereby no weaker side exists.

69. The device as in claim 66 in which the solid state material layer is formed using real-time monitoring and closed-loop feedback control to achieve a precision of one to several atoms on a material layer dimension selected from the group consisting of thickness, depth, curvature, shape, size, chemical composition profiling, and lateral location.

70. The device as in claim 66 in which at least a portion of the solid state material layer is bonded to the substrate with an initially liquid bonding material;

the liquid bonding material wetting and filling surface defects on the solid state material layer and then solidifying and converting these liquid-filled surface defects into solid reinforcements, whereby the bonded material layer is stronger than the unbonded solid state material itself.

71. The device as in claim 66 in which the solid state material layer is sufficiently thin and flexible so as to yield significantly thereby preventing device failures through a curvature-related stress-relieving and strain-relieving mechanism .

72. The device as in claim 66 in which the solid state material layer is formed at least partly by laser heating to melt the solid state material layer; and including controllably solidifying the melted layer material into a liquid-diffusion aged, solid state material layer.

73. The device as in claim 66 having a thickness of less than a micron to one atomic layer thereby forming a thin-film integrated circuit device.

74. The device as in claim 66 wherein the solid state material layer is curved with a radius of curvature of less than a value selected from the group consisting of 0.5 microns and 1 micron.

75. The device as in claim 66 in which the solid state material layer is made by a melting and solidification process;

the purity of material of the layer being improved due to the melting and solidification by at least one order of magnitude based on a segregation coefficient

according to a relevant alloy phase diagram.

76. Th device as in claim 66 in which the solid state material layer has at least one atomically smooth major surface produced by an atomic smoothing process.

77. The device as in claim 66 in which the solid state material layer is made by ion implantation under 1 kilovolt of implanting voltage to achieve a depth accurate to atomic layers .

78. A solid state device as in claim 66 including:

a first and a second solid state material pockets positioned adjacent to, but laterally separated by a gap, on the top surface of the substrate;

the solid state material layer thereby bridging the gap between the two adjacent solid state material pockets; and

at least a portion of the solid state material layer having an accuracy in thickness of no more than three atomic layers and being uniformly bonded uniformly to at least a selected area of the substrate avoiding imperfectly bonding interfacial region.

79. A solid state device as in claim 78 in which:

at least a part of the substrate is a semiconductor of a first conductivity type; and

at least one of the semiconductor pockets is of a second conductivity type forming at least one PN junction region where the part of the substrate contacts the at least one semiconductor material pocket.

80. The device as in claim 66 in which the solid state material layer is selected from the group consisting of a gate layer and a field layer.

81. The device as in claim 66 in which the substrate material is selected from the group consisting of Si, Ge, Si-Ge, InP, InSb, GaAs, SiC, InAs, superconductor, diamond, semiconductor material, intrinsic semiconductor material, substantially electrically insulating material, and substantially electrically conducting material, and mixture thereof.

82. The device as in claim 66 selected from the group consisting of metal-oxide-semiconductor (MOS) device, and conductor-insulator-semiconductor (CIS) device, thin-film integrated circuit, and flexible integrated circuit.

83. The device as in claim 66 in which:

th solid state material pockets are respectively source and drain semiconductor pockets in a CMOS device;

the solid state material layer is a gate layer bridging the two pockets;

the gate layer material is laser heated and melted to smooth at least one of the top and bottom surfaces by an atomic surface-smoothing mechanism; and

solidification of the molten gate layer material, sub-layer by sub-layer from the bottom surface up, purifies the gate layer material greatly reducing impurities and improving insulation most at a surface contacting the substrate.

84. The device as in claim 66 in which at least a major portion of the substrate, solid state material pockets, solid state material layer, and electrical contacts are selected to consist essentially of a single intrinsic doped and less doped semiconductor material whereby the device is made resistant to dynamic forces due to impacts, vibrations, and large and rapid accelerations and decelerations, because the plurality of the selected device component materials have practically the same density and differ from each other by only ppm or ppb of impurities.

85. The device as in claim 66 including a PN junction region having a curved adjoining surface and provided on the substrate; and

at least one of inevitable thermal mismatch stress and in situ volume change strain generated during device processing being reduced but not eliminated, through a curvature-related strain-relieving and stress-relieving mechanism operating on the curved adjoining surface;

the remaining residual strain and stress on the curved adjoining surface of the PN junction region being utilized to improve a device performance.

86. The device as in claim 79 in which:

the substrate is a semiconductor of one conductivity type and has a matching part contacting the curved adjoining surface of the PN junction region;

at least one of the first and second solid state material pockets is a semiconductor of the opposite conductivity type thereby forming at least one PN junction region where the substrate meets the curved adjoining portion of the at least

one solid state material pocket;

the PN junction region is within 40 atomic layers from the substrate ; and

the stresses and strains are reduced, but not completely eliminated, by a curvature-related stress-relieving mechanism; and

the remaining stresses and strains still provide sufficient stresses and strains to favorably affect characteristics of the PN junction region.

87. The device as in claim 66 in which the solid state material layer has been superficially ion-implanted with dopants in high concentrations therein;

the superficially ion-implanted layer being rapidly laser spike melted to have superficial liquidisation and a very shallow, highly activated doped region due to the high spike heating rates allowing much greater dopant concentrations than the thermal equilibrium phase-diagram values.

88. The device as in claim 66 in which the solid state material layer is an electrically insulating, wavy and curved field layer formed by at least partly ion-implanting with an ion-implanting beam into a silicon material substrate a substance selected from the group consisting of oxygen and nitrogen;

at least one of the substrate and the ion-implanting beam having a wavy and curved movement relative to the other during the ion-implanting process to produce the wavy and curved field layer.

89. The device as in claim 66 in which:

the solid state material pockets are respectively source and drain semiconductor pockets in a CMOS device; and

the solid state material layer is a gate layer bridging the gap between the two pockets; and

including a conductive gate electrode formed of an electrically conducting material and generally centered on the gate layer to control flow of electronic carriers from the source to the drain.

90. The device as in claim 89 in which:

a laser heating beam melts the gate layer material and smooths at least one of

top and bottom major surfaces by an atomic surface-smoothing mechanism achieving maximum smoothness; and

solidification of the molten gate layer material, sub-layer by sub-layer from the bottom surface up, purifies the gate layer material greatly reducing impurities and improving insulation most at the bottom surface facing the substrate.

91. The solid state device as in claim 66 in which:

the solid state material layer is a field layer separating and electrically isolating device components from each other;

the field layer on a horizontal cross-section thereof has a plurality of curved sections; and

each curved section has an arc length defined by: l = r x A where l is the arc length, r is the radius of curvature of the arc, and A is the subtended arc angle;

each arc section being capable of flexing whereby the arc length is changed by delta l = r x delta A + A x delta r; and

the changes in delta l, delta r, and delta A all being in directions to reduce thermal mismatch strain and automatically stopping when the residual mismatch strain is reduced by the changing arc length to a point such that the multiply curved field layer can tolerate without failure the residual thermal mismatch strain.

92. The solid state device as in claim 66 in which the solid state material layer is curved to minimize thermal mismatch stresses through a curvature-related strain-relieving and stress-relieving mechanism.

93. A mass-produced solid state device comprising:

a solid state material substrate;

at least one first solid state material pocket positioned on a first selected surface of the substrate; and

a solid state material layer having at least one atomically smooth major surface which contacts and metallurgically perfectly bonds uniformly the first selected surface of the substrate to a first specified portion of the at least one first solid state material pocket.

94. A solid state device as in claim 93 further comprising:

a second solid state material pocket positioned on a second selected surface of the substrate, and laterally adjacent to, but separated by a gap from, the at l ast one first solid state material pocket; and in which:

the solid state material layer fills the gap between the two material pockets while contacts and metallurgically perfectly bonds uniformly with a second specified portion of the second solid state material pocket; and

the solid state material layer is mechanically perfect and is no more than 3 to 40 Angstroms thick.

95. A mass-produced solid state device comprising:

a solid state material substrate;

a left and a right adjacent solid state material pockets laterally separated by a gap and positioned on a common top surface of the substrate;

a curved solid state material layer which: a) has a radius of curvature of no more than 1.0 micron; and b) is positioned on the top surface of the substrate to bridge the gap between the two solid state material pocket; and

at least a portion of the solid state material layer being metallurgically continuously bonded to at least a selected area of the top surface of the substrate with a mechanically perfect bonding interfacial region to avoid imperfectly bonded material layer leading to poor device yield, performance, reproducibility, reliability, and life.

REMARKS

Applicant elects the Group II claims 25-47 and 58-60, drawn to Semiconductor Device, classified in class 257, subclass 509. Claims 1-24, 48-57, and 61-65 are removed from this case without prejudice. An early action on the merits is respectfully requested

Any fee not covered by the attached check necessary to effect entry of this amendment should be charged to the undersign's deposit account 50-1770.

In view of the amendments and remarks above, Applicants submit that this application is in condition for allowance and request reconsideration and favorable action thereon.

Respectfully submitted,

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Enclosures: EOT three months
Abstract of the Disclosure
Drawing changes

The undersigned certifies that this amendment was filed on by facsimile and transmitted to the USPTO to 703 872-9318 on June 27, 2002

James A. Poulos, III Date: June 27, 2002